Attorney Docket: 012.P53015

AMENDMENT

IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer, and Assignee reserves the right to claim this subject matter in a continuing application:

1. (Currently Amended) A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress points;

a first buffering structure, coupled to a first one of said ingress/egress ~~point~~ points and a first one of said mediums, including a first FIFO storage structure to stage ~~undiverted ones of~~ a first plurality of egress packets, and ~~first undiverted egress packet drop logic coupled to the first FIFO storage structure to selectively effectuate head or tail flushes of said first FIFO storage structure~~ packet diversion and insertion logic to enable post-switching pre-medium diversion and insertion of egress packets on the first one of said mediums; and

a second buffering structure, coupled to a second one of said ingress/egress ~~point~~ points and a second one of said mediums, including a second FIFO storage structure to stage ~~undiverted ones of a~~ second plurality of egress packets, and ~~second undiverted egress packet drop logic coupled to the second FIFO storage structure to selectively effectuate head or tail flushes of said second FIFO storage structure~~ packet diversion and insertion logic to enable post-switching pre-medium diversion and insertion of egress packets on the second one of said mediums.

2. (Currently Amended) The apparatus of claim 1, ~~wherein said first undiverted egress packet drop logic comprises~~ further comprising ~~first undiverted~~ egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an egress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first ~~FIPO~~ FIFO storage structure.

3. (Currently Amended) The apparatus of claim 1, ~~wherein said first undiverted egress packet drop logic comprises~~ further comprising ~~first undiverted~~ egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first ~~FIPO~~ FIFO storage structure.

4. (Currently Amended) The apparatus of claim 3, wherein said ~~first undiverted~~ egress packet write drop logic further sets a bad egress packet bit to denote for a downstream processor that an immediately preceding egress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

5. (Currently Amended) The apparatus of claim 1, ~~wherein said first undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an egress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is greater than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and if so, reloads a write pointer associated with the first~~

~~FIFO storage structure with an address that is of a second predetermined distance from the SOP of the egress packet to be dropped, and~~

~~writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure~~ further comprising a processor interface coupled to each of the first and the second buffering structures, to respectively enable communication between the first and the second buffering structures and a first and second processor.

6. (Currently Amended) The apparatus of claim [[1]]5, wherein said first ~~undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an egress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is less than a read pointer associated with the first FIFO storage structure by a first predetermined distance, if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and~~

~~writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure~~ and second processors comprise Application Specific Integrated Circuits (ASICs).

7. (Currently Amended) The apparatus of claim 1, wherein said ~~first undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an egress packet to be dropped is no longer in the first FIFO storage structure, and if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a first predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and~~

~~writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure~~ diversion and insertion are performed during data link/physical layer processing of egress packets.

8. (Currently Amended) The apparatus of claim 1, ~~wherein said first undiverted egress packet drop logic comprises~~ further comprising ~~first undiverted~~ egress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol, multiplexes an EOP into said first plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said first FIPO storage structure.

9. (Currently Amended) The apparatus of claim [[1]]7, wherein said ~~first undiverted egress packet drop logic comprises first undiverted egress packet read drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an egress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating remaining words of the egress packet, to effectuate a head flush of said first FIPO storage structure~~ diversion and insertion and said data link/physical layer processing of egress packets are performed by a single Application Specific Integrated Circuit (ASIC).

10-24. (Cancelled)

25. (Currently Amended) A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress;

a first buffering structure, coupled to a first one of said ingress/egress points and a first of said mediums, including a first FIFO storage structure to stage ~~undiverted ones of~~ a first plurality of ingress packets, and ~~first undiverted ingress packet drop logic coupled to the first FIFO storage structure to~~

~~selectively effectuate head or tail flushes of said first FIFO storage structure~~ packet diversion and insertion logic to enable post-medium extraction, pre-switching diversion and insertion of egress packets on the first one of said mediums; and

a second buffering structure, coupled to a second one of said ingress/egress points and a second of said mediums, including a second FIFO storage structure to stage ~~undiverted ones of~~ a second plurality of ingress packets, and ~~second undiverted ingress packet drop logic coupled to the second FIFO storage structure to selectively effectuate head or tail flushes of said second FIFO storage structure~~ packet diversion and insertion logic to enable post-medium extraction, pre-switching diversion and insertion of egress packets on the second one of said mediums.

26. (Currently Amended) The apparatus of claim 25, ~~wherein said first undiverted ingress packet drop logic comprises~~ further comprising ~~first undiverted~~ ingress packet write drop logic, which, in response to an overflow condition of said third FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an ingress packet being dropped, and writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first ~~FIPO~~ FIFO storage structure.

27. (Currently Amended) The apparatus of claim 25, ~~wherein said first undiverted ingress packet drop logic comprises~~ further comprising ~~first undiverted~~ ingress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

28. (Currently Amended) The apparatus of claim 27, wherein said ~~first undiverted~~ ingress packet write drop logic further sets a bad ingress packet bit to denote for a system-side interface that an immediately preceding ingress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

29. (Currently Amended) The apparatus of claim 25, ~~wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is greater than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and if so,~~

~~reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from the SOP of the ingress packet to be dropped, and~~

~~writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure~~ further comprising a processor interface coupled to each of the first and the second buffering structures, to respectively enable communication between the first and the second buffering structures and a first and second processor.

30. (Currently Amended) The apparatus of claim 25, wherein said first ~~undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is less than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and if so,~~

~~reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and~~

~~writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure~~ and second processors comprise Application Specific Integrated Circuits (ASICs).

31. (Currently Amended) The apparatus of claim 25, wherein said ~~first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an ingress packet to be dropped is no longer in the first FIFO storage structure, and if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a first predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and~~

~~writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure~~ diversion and insertion are performed during data link/physical layer processing of ingress packets.

32. (Currently Amended) The apparatus of claim 25, ~~wherein said first undiverted ingress packet drop logic comprises~~ further comprising ~~first undiverted~~ ingress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol,

multiplexes an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure.

33. (Currently Amended) The apparatus of claim 25, wherein said ~~first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and if so, invalidating remaining words of the ingress~~

~~packet to be dropped, to effectuate a head flush of said first FIFO storage structure~~ diversion and insertion and said data link/physical layer processing of ingress packets are performed by a single Application Specific Integrated Circuit (ASIC).

34. (Cancelled)~~The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an ingress packet to be dropped has already been read out of the first FIFO storage structure, and if so, invalidating an EOP indicator of a current word, to effectuate a head flush of said first FIFO storage structure~~

35-36. (Cancelled)

37. (Currently Amended) A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch packets received through mediums coupled to the ingress/egress points; and

a buffering structure including a first FIFO storage structure, coupled to a first of said ingress/egress points and a first of said mediums, to stage ~~undiverted ones of~~ a first plurality of ingress packets, and ~~undiverted ingress packet drop logic to selectively effectuate head or tail flushes of said first FIFO storage structure, and a second FIFO storage structure, coupled to said first ingress/egress point and said first of said mediums, to stage undiverted ones of a first plurality of egress packets, and undiverted egress packet drop logic to selectively effectuate head or tail flushes of said second FIFO storage structure~~ packet diversion and insertion logic to enable post-medium extraction, pre-switching diversion and insertion of egress packets on the first one of said mediums, and to enable post-switching pre-medium diversion and insertion of egress packets on the first one of said mediums.

38. (Currently Amended) The apparatus of claim 37, ~~wherein said undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure, while operating under a first protocol, reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an ingress packet being dropped, and writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure~~ further comprising a processor interface coupled to each of the first and the second buffering structures, to respectively enable communication between the first and the second buffering structures and a first and second processor.

39. (Currently Amended) The apparatus of claim 37, wherein said ~~undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,~~

~~reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure~~ diversion and insertion are performed during data link/physical layer processing of egress packets.

40. (Currently Amended) The apparatus of claim 39, wherein said ~~undiverted ingress packet write drop logic further sets a bad ingress packet bit to denote for a system side interface that an immediately preceding ingress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer~~ diversion and insertion and said data link/physical layer processing of egress packets are performed by a single Application Specific Integrated Circuit (ASIC).

41. (Currently Amended) The apparatus of claim 37, wherein said ~~undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is greater than a read pointer associated with the first FIFO storage structure by a first predetermined distance, if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from the SOP of the ingress packet to be dropped, and writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure~~ diversion and insertion are performed during data link/physical layer processing of ingress packets.

42. (Currently Amended) The apparatus of claim 37, wherein said ~~undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,~~

~~determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is less than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIFO storage structure~~ diversion and insertion and said data link/physical layer processing of ingress packets are performed by a single Application Specific Integrated Circuit (ASIC).

43-59. (Cancelled)

60-79. (Withdrawn)

80. (New) An apparatus, comprising:

means for diverting egress packets from a transmit path into a buffer during data link/physical layer processing of egress packets on the transmit path; and

means for inserting egress packets into a transmit path during data link/physical layer processing of egress packets on the transmit path.

81. (New) The apparatus of claim 80, further comprising:

means for selectively flushing buffered packets from the buffer.

82. (New) The apparatus of claim 81, wherein means for selectively flushing comprises means for head and/or tail flushing of the buffered packets.

83. (New) An apparatus, comprising:

means for diverting ingress packets from a transmit path into a buffer during data link/physical layer processing of ingress packets on the transmit path; and

means for inserting ingress packets into a transmit path during data link/physical layer processing of ingress packets on the transmit path.

84. (New) The apparatus of claim 83, further comprising:

means for selectively flushing buffered packets from the buffer.

85. (New) The apparatus of claim 84, wherein means for selectively flushing comprises means for head and/or tail flushing of the buffered packets.

86. (New) A buffering structure, comprising:

a plurality of egress packet storage structures;

egress packet divert logic to selectively perform post-medium, pre-insertion diversion of egress packets from a transmit path to one of the egress packet storage structures; and

egress packet insert logic to selectively perform post-medium, pre-insertion insertion of one or more egress packets from the egress packet storage structure to a transmit path, wherein the diversion and insertion are performed during data link/physical layer processing of the egress packets.

87. (New) The buffering structure of claim 86, wherein the egress packet storage structures further comprise:

at least one egress undiverted packet storage structure;

at least one egress diverted packet storage structure; and

at least one egress insert packet storage structure.

88. (New) The buffering structure of claim 87, wherein the egress packet divert logic is adapted to selectively perform post-medium, pre-insertion diversion of egress packets from a transmit path to at least one egress diverted packet storage structure.

89. (New) The buffering structure of claim 87, wherein the egress packet insert logic is adapted to selectively perform post-medium, pre-insertion insertion of one or more egress packets from one or more of the at least one egress undiverted packet storage structure and the at least one egress insert packet storage structure.

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